UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,533	10/12/2000	Motoshi Ito	YAMAP0741US	9029

7590 07/16/2003

Neil A DuChez
Renner Otto Boisselle & Sklar LLP
1621 Euclid Avenue
19th Floor
Cleveland, OH 44115

EXAMINER	
LI, ZHUO H	
ART UNIT	**PAPER NUMBER**
2186	6

DATE MAILED: 07/16/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/689,533	Applicant(s) ITO ET AL.	
	Examiner Zhuo H Li	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on October 12, 2000 (Paper no. 5) has been considered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 32 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 32, the term "I/F control" on line 3 is unclear what kind of controlling operation.

The following art rejections are applied from what is best understood of the clam in view of the 112 Second paragraph problems listed above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-3, 5-6, 8-9, 12, 14-18, 21, 23-25 and 27-28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US PAT. 5,504,701 hereinafter Takahashi).

Regarding claim 1, Takahashi discloses an information update count, i.e., a flash erase EEPROM (100, figure 1) managing method which comprising a wired logic circuit wherein the wired logic circuit is for controlling read, write and erase operation for a number of memory cells, i.e., sectors constituting the memory (100, figure 1), the number of memory cells stored a predetermined of data and is able to rewritten, i.e., erased, in sequence by a user terminal device (col. 2 line 55 through col. 3 line 3), and the memory receives commands via the command decoder (20) wherein the commands include an instruction code, an address, a data length, and a data, i.e., a word including a plurality of bits (col. 3 lines 4-26). Although Takahashi does not clearly teaches the information update count further comprising a step of reading out a last piece of information which has been written in the information storage area within a predetermined permitted update count, Takahashi merely teaches the read/write control logic (110) is capable to

controlling a reading operation for each memory cell of the flash memory (100) (col. 3 lines 45-51), in addition, Takahashi gives a example of a prepaid telephone call, i.e. flash memory, is capable to read, write and erase wherein when data of all the memory cells are rewritten, the prepaid card can not be used any more, i.e., a predetermined permitted update count. Thus, Takahashi teaches the read/write control logic (110) reads the information from the flash memory based upon the updated data/address in the memory cells, i.e., counting the number of times the memory is initialized/erased, (col. 3 line 27 through col. 4 line 8). It recognizes Takahashi teaches the read out a last piece of information which has been written in the information storage area within a predetermined permitted update count, because it prevented the memory from being initialized (reused) over a predetermined number of times and can be prevented from being used dishonestly without restriction.

Regarding claim 2, Takahashi teaches an information updated count managing method further comprising an erase step of erasing all of the bits of all of the words in the sector including the information storage area (col. 3 lines 27-45 and col. 4 lines 8-49).

Regarding claim 3, Takahashi teaches an information update count managing method further comprising an erase step of erasing step of setting all of the bits of all of the words in each sector to "1" (col. 2 line 55 through col. 3 lines 3).

Regarding claim 5, Takahashi teaches an information update count managing method wherein the predetermined order is an ascending order of addresses of the words (col. 2 line 55 through col. 3 line 3, col. 3 lines 36-45 and col. 4 line 63 through col. 5 line 8).

Regarding claim 6. Takahashi teaches an information update count managing method wherein an upper limit value of the predetermined permitted update count is determined based on

the number of words in the information storage area, i.e., user memory (100) is able to programmed with different predetermined permitted update count by the user terminal device or manufactory (col. 2 line 55 through col. 3 line 3 and col. 4 line 52 through col.5 line 8).

Regarding claims 8 and 9, Takahashi teaches an information update count managing method wherein the write step comprising a step of writing one or more of the plurality of bits in the at least one word from "1" to "0" (col. 2 line 55 through col. 3 line 3, col. 4 lines 52-62 and col. 6 lines 28-46), and the read step comprises a step of reading out, as the last piece of information which has been written in the information storage area within the predetermined permitted updated count, a last hit word found in a search through the information storage area for words in which at least one bit is "0", the words in the information storage area being searched through in the predetermined order (col. 3 line 27 through col. 4 line 8 and col. 6 line 53 through col. 7 line 42), the write step comprise a step of writing one bit in the at least on word from "1" to "0" and the read step comprises a step of determining the information of a word in which two or more bits are "0" to be invalid (col. 2 line 55 through col. 3 line 3 and col.3 lines 37-45).

Regarding claim 12, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 14, the limitations of the claim are rejected as the same reasons set forth in claim 5.

Regarding claim 15, the limitations of the claim are rejected as the same reasons set forth in claim 6.

Regarding claim 16, the limitations of the claim are rejected as the same reasons set forth in claim 7.

Regarding claims 17-18, the limitations of the claim are rejected as the same reasons set forth in claims 8-9.

Regarding claim 21, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claims 23-24, Takahashi teaches an information update count managing method wherein the contents usage count is read out as the number of remaining times or as the number of times the content can be used (col. 3 line 37 through col. 4 line 8 and col. 6 line 53 through col. 7 line 42).

Regarding claim 25, the limitations of the claim are rejected as the same reasons set forth in claim 1.

Regarding claim 27-28, the limitations of the claim are rejected as the same reasons set forth in claims 23-24.

7. Claims 4, 7, 10-11, 13, 19-20, 22, 26 and 29-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takahashi et al. (US PAT. 5,504,701 hereinafter Takahashi) as applied to claims above, and further in view of Kon (US PAT. 6,249,838).

Regarding claim 4, Takahashi differs from the claimed invention in not specifically teaches the information update count managing method wherein the information storage area is provide in a same sector as an initialization operation program which is a first program to be executed after a reset. However, Kon teaches in the data storage unit, i.e., flash memory (212,

figure 2) comprising a memory array, i.e., information storage area, which including a plurality of memory cells, i.e., memory sectors, a REL logic (226, figure 2) which stores information from which remaining-expected-lifetime information can be determined or derived of each memory cell (col. 5 lines 23-35), and counter (232, figure 2) in a header area of each memory cell has stored in it an initial value indicative of the maximum number of permissible erasures for the flash memory (col. 6 line 36 through col. 7 line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the flash memory of Takahashi in having a step of the information storage area is provide in a same sector as an initialization operation program which is a first program to be executed after a reset, as per teaching of the flash memory by Kon, because it prevents further access, such as read, write and erase after the storage devices is over/reached the predetermined count.

Regarding claim 7, Takahashi differs from the claimed invention in not specifically teaches the information update count managing method wherein the pieces of information include regional information which is used for controlling a region where a content can be reproduced. However, Kon teaches in the data storage unit, i.e., flash memory (212, figure 2) comprising a memory array, i.e., information storage area, which including a plurality of memory cells, i.e., memory sectors, a REL logic (226, figure 2) which stores information from which remaining-expected-lifetime information can be determined or derived of each memory cell (col. 5 lines 23-35), and counter (232, figure 2) in a header area of each memory cell has stored in it an initial value indicative of the maximum number of permissible erasures for the flash memory (col. 5 line 27 through col. 6 line 2 and col. 6 line 36 through col. 7 line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the

invention was made to modify the flash memory of Takahashi in having the pieces of information include regional information which is used for controlling a region where a content can be reproduced, as per teaching of the flash memory by Kon, because it prevents further access, such as read, write and erase after the storage devices is over/reached the predetermined count.

Regarding claim 10, Takahashi differs from the claimed invention in not specifically teaches the method wherein the write step comprises a step of storing in an update count storage area, the number of times information has been written in the information storage area. However, Kon teaches in the data storage unit, i.e., flash memory (212, figure 2) comprising a memory array, i.e., information storage area, which including a plurality of memory cells, i.e., memory sectors, a REL logic (226, figure 2) which stores information from which remaining-expected-lifetime information can be determined or derived of each memory cell (col. 5 lines 23-35), the REL in corporate with counter (232, figure 2) calculating and determining whether each memory cell reach it's predetermine amount of times or erasures. In addition, Kon teaches the flash memory is able to updated/store the updated information, such as erasure times of each memory cell (col. 6 line 36 through col. 7 line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the flash memory of Takahashi in having a step of storing in an update count storage area, the number of times information has been written in the information storage area, as per teaching of the flash memory by Kon, because it prevents further access, such as read, write and erase after the storage devices is over/reached the predetermined count.

Regarding claim 11, Kon teaches an information update count managing wherein the update count storage area is in the same sector as an initialization operation program which is a first program to be executed after a reset (col. 6 line 36 through col. 7 line 59).

Regarding claim 13, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 19, the limitations of the claim are rejected as the same reasons set forth in claim 10.

Regarding claim 20, the limitations of the claim are rejected as the same reasons set forth in claim 11.

Regarding claim 22, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 26, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Regarding claim 29, Takahashi teaches an information update count, i.e., flash memory (100, figure 1) managing method which comprising a wired logic circuit wherein the wired logic circuit is for controlling read, write and erase operation for a number of memory cells, i.e., sectors constituting the memory (100, figure 1), the number of memory cells stored a predetermined of data and is able to rewritten, i.e., erased, in sequence by a user terminal device (col. 2 line 55 through col. 3 line 3), and the memory receives commands via the command decoder (20) wherein the commands include an instruction code, an address, a data length, and a data, i.e., a word including a plurality of bits (col. 3 lines 4-26). Although Takahashi does not clearly teaches the information update count further comprising a step of reading out a last piece

of information which has been written in the information storage area within a predetermined permitted update count, Takahashi merely teaches the read/write control logic (110), i.e., micro processor, is capable to controlling a reading operation for each memory cell of the flash memory (100) (col. 3 lines 45-51), in addition, Takahashi gives a example of a prepaid telephone call, i.e. flash memory, is capable to read, write and erase wherein when data of all the memory cells are rewritten, the prepaid card can not be used any more, i.e., a predetermined permitted update count. Thus, Takahashi teaches the read/write control logic (110) reads the information from the flash memory based upon the updated data/address in the memory cells, i.e., counting the number of times the memory is initialized/erased, (col. 3 line 27 through col. 4 line 8). It recognizes Takahashi teaches the read out a last piece of information which has been written in the information storage area within a predetermined permitted update count, because it prevented the memory from being initialized (reused) over a predetermined number of times and can be prevented from being used dishonestly without restriction. However, Takahashi differs from the claimed invention in not specifically teaches the information update count managing apparatus wherein the non-volatile memory includes a boot area and a system area each including one or more sectors. However, Kon teaches in the computer system (114, figure 1) comprising a CPU (126, figure 2) and a data storage unit (112, figure) wherein the storage unit comprising a memory array, i.e., system area, which including a plurality of memory cells, i.e., memory sectors, a REL logic (226, figure 2), i.e., boot area which stores information from which remaining-expected-lifetime information can be determined or derived of each memory cell (col. 5 lines 23-35), the REL in corporate with counter (232, figure 2) calculating and determining whether each memory cell reach it's predetermine amount of times or erasures. In addition, Kon

teaches the flash memory is able to updated/store the updated information, such as erasure times of each memory cell (col. 6 line 36 through col. 7 line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the flash memory of Takahashi in having a boot area and a system area each including one or more sectors, as per teaching by the system of Kon, because it prevents further access, such as read, write and erase after the storage devices is over/reached the predetermined count.

Regarding claim 30, Kon teaches an information update count managing apparatus wherein the boot area further comprises a check program, i.e., counter (232) for checking contents of the information storage area (col. 5 line 27 through col. 6 line 2).

Regarding claim 31, Kon teaches an information update count managing apparatus wherein immediately after the micro processor unit is reset, the micro processor unit executes the micro processor unit initialization program and then the check program, and then the program stored in the system area (col. 6 line 36 through col. 7 line 59).

Regarding claim 32, Kon teaches an information update count managing apparatus wherein the boot area further comprises I/F control means for receiving a program to be stored in the system area from an upper control unit which is connected to the information update count managing apparatus (col. 5 line 27 through col. 6 line 2 and col. 6 line 36 through col. 7 line 59).

Regarding claim 33, Kon teaches an information update count managing apparatus wherein the boot area further comprises flash memory update means for updating a program in the system area (col. 7 line 60 through col. 9 line 12).

Regarding claim 34, Kon discloses an information update count managing apparatus wherein immediately after the micro processor unit is reset, the micro processor unit executes the

micro processor unit initialization program, and then waits for reception from the upper control nit which is connected to the information update count managing apparatus (col. 7 line 60 through col. 9 line 12).

Regarding claim 35, Kon discloses an information update count managing apparatus wherein the micro processor unit calls a program in the boot area from a grogram in the system area (col. 5 line 27 through col. 6 line 35).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Davis (US PAT. 5,963,970) discloses method and apparatus for tracking erase cycles utilizing active and inactive wear bar blocks having first and second count fields (abstract).

Kynett et al. (US PAT. 5,513,333) discloses circuitry and method for programming and erasing a non-volatile semiconductor memory (col. 2 lines 36-63).

Sawabe et al. (US PAT. 6,122,434) discloses information recording medium, having data and management portions, and an apparatus for reproducing information from the medium (abstract).

9. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7239

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

Art Unit 2186

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100